

**IN THE CLAIMS**

Please cancel claims 16, 27, 29 and 36 without prejudice or disclaimer, and amend claims 1, 17 and 28, as follows:

1       1. (Currently Amended) An apparatus, comprising:

2           a converter for converting an input optical signal to an original electrical signal;

3           an identification unit for receiving said original electrical signal, for generating a

4       first signal comprising said original electrical signal delayed by a predetermined quantity

5       of time, for generating a second signal comprising said original electrical signal not

6       delayed, for comparing said first and second signals, for forming a third signal in

7       dependence upon said comparing of said first and second signals, and for detecting a bit

8       rate in dependence upon said third signal;

9           a clock generator for generating a separate reference clock signal in dependence

10       upon said detected bit rate; and

11           a recovery unit for recovering an input clock signal and data from said input

12       optical signal in dependence upon said reference clock signal;

13           wherein said clock generator comprises a plurality of oscillators for generating  
14           clocking signals of different frequencies, said oscillators being selectively operated to  
15           generate said reference clock signal in dependence upon said bit rate detected by said  
16           identification unit; and

17           wherein said identification unit further comprises:

18           a first unit for delaying said original electrical signal, for performing an exclusive  
19       -OR operation upon said first and second signals, and for forming said third signal in  
20       dependence upon said exclusive-OR operation performed upon said first and second  
21       signals; and

22           a second unit for low-pass filtering said third signal, and for detecting said bit rate  
23       directly from a voltage level of said low-pass filtered third signal and without using a  
24       phase locked loop;

25           said second unit comprising:

26           a low-pass filter for low-pass filtering said third signal;  
27           an analog-to-digital converter for receiving said low-pass filtered third  
28       signal, and for converting said low-pass filtered third signal from an analog signal  
29       to a digital signal; and

30           a bit rate deriving unit for deriving said bit rate directly from a voltage level  
31       of said digital signal received from said analog-to-digital converter.

32       2. (Previously Presented) The apparatus of claim 1, said apparatus comprising an  
33       optical receiver for receiving optical signals having a plurality of different bit rates.

1       3. (Previously Presented) The apparatus of claim 1, said bit rate of said input  
2       optical signal comprising a transmission rate.

1       4. (Previously Presented) The apparatus of claim 1, further comprising an  
2       amplifier for amplifying said original electrical signal received from said converter.

1       5. (Original) The apparatus of claim 4, said amplifier outputting said amplified  
2       electrical signal to said identification unit.

1       6. (Previously Presented) The apparatus of claim 1, said converter comprising an  
2       optoelectric converter.

1       7. (Previously Presented) The apparatus of claim 1, said identification unit  
2       comprising a bit rate identification unit.

1       8. (Previously Presented) The apparatus of claim 1, said comparing performed by  
2       said identification unit comprising said identification unit performing an exclusive-OR  
3       logic operation upon said first and second signals.

Claims 9 - 11. (Cancelled)

1       12. (Previously Presented) The apparatus of claim 1, said first unit comprising a  
2       bit rate identification signal generator.

1        13. (Previously Presented) The apparatus of claim 1, said second unit comprising  
2        a bit rate deriving unit.

Claim 14. (Cancelled)

1        15. (Previously Presented) The apparatus of claim 1, said first unit comprising:  
2        a buffer unit for receiving said original electrical signal, and for outputting two  
3        duplicate signals substantially equivalent to said original electrical signal, said two  
4        duplicate signals comprising a primary signal and a secondary signal;  
5        a delay unit for receiving said primary signal, for delaying said primary signal by  
6        said predetermined quantity of time, and for outputting said delayed primary signal, said  
7        delayed primary signal comprising said first signal and said secondary signal comprising  
8        said second signal; and  
9        an operator unit for performing said exclusive-OR logic operation upon said first  
10      and second signals.

Claim 16. (Canceled)

1        17. (Currently Amended) A method of operating a receiver which functions  
2        independently of a bit rate of a received signal, comprising:  
3        receiving an original signal;

4 generating a resultant signal by performing an exclusive-OR operation on a first  
5 signal and a second signal, said first signal comprising said original signal delayed by a  
6 predetermined quantity of time, said second signal comprising said original signal not  
7 delayed;

8 determining a bit rate of said original signal by low-pass filtering said resultant  
9 signal and without using a phase locked loop, and deriving said bit rate directly from a  
10 voltage level of the low-pass filtered resultant signal and without using said phase locked  
11 loop;

12 generating a reference clock signal separate from said original signal and in  
13 dependence upon said determined bit rate; and

14 recovering an input clock signal and data from said original signal in dependence  
15 upon said reference clock signal;

16 said generating of said reference clock signal being performed by a clock  
17 generator, said clock generator comprising a plurality of oscillators for generating  
18 clocking signals of different frequencies, and said oscillators being selectively operated  
19 to generate said reference clock signal in dependence upon said detected bit rate.

Claim 18. (Cancelled)

1 19. (Previously Presented) The method of claim 17, said original signal  
2 comprising an input optical signal, said method further comprising:

3                   converting said input optical signal to an electrical signal;  
4                   outputting two duplicate signals substantially equivalent to said electrical signal,  
5                   said two duplicate signals comprising a primary signal and a secondary signal; and  
6                   delaying said primary signal by said predetermined quantity of time, and  
7                   outputting said primary signal, said delayed primary signal comprising said first signal.

1                   20. (Previously Presented) The method of claim 17, said first and second signals  
2                   comprising electrical signals.

1                   21. (Previously Presented) The method of claim 17, said method comprising  
2                   receiving signals having a plurality of different bit rates.

1                   22. (Previously Presented) The method of claim 17, said original signal received  
2                   comprising a plurality of original signals received, said recovering of said input clock  
3                   signal and data from said original signal being performed for said plurality of original  
4                   signals received, said plurality of original signals received having a respective plurality  
5                   of different bit rates.

1                   23. (Original) The method of claim 17, said recovering of said input clock signal  
2                   and data from said original signal being performed for a plurality of original signals  
3                   received, said plurality of original signals received having a respective plurality of

4 different bit rates.

1 24. (Previously Presented) The method of claim 17, said method comprising  
2 receiving optical signals having a plurality of different bit rates.

1 25. (Previously Presented) The method of claim 17, further comprising:  
2 receiving an input optical signal;  
3 converting said input optical signal to an original electrical signal;  
4 outputting two duplicate signals substantially equivalent to said original electrical  
5 signal, said two duplicate signals comprising a primary signal and a secondary signal; and  
6 delaying said primary signal by said predetermined quantity of time, and  
7 outputting said primary signal, said delayed primary signal comprising said first signal,  
8 said outputted primary signal comprising said second signal.

1 26. (Previously Presented) The method of claim 17, said receiving of said original  
2 signal being performed by an optoelectric converter, said original signal being an optical  
3 signal, said optoelectric converter converting said original optical signal to an electrical  
4 signal, said method further comprising:

5 outputting two duplicate signals substantially equivalent to said electrical signal,  
6 said two duplicate signals comprising a primary signal and a secondary signal, said  
7 outputting of said two duplicate signals being performed by a buffer; and

8           delaying said primary signal by said predetermined quantity of time, and  
9        outputting said primary signal, said delayed primary signal comprising said first signal,  
10      and said outputted primary signal comprising said second signal.

Claim 27. (Canceled)

1           28. (Currently Amended) An apparatus, comprising:  
2           a converter for converting an input optical signal to an original electrical signal;  
3           an identification unit for receiving said original electrical signal, for generating a  
4        first signal comprising said original electrical signal delayed by a predetermined quantity  
5        of time, for generating a second signal comprising said original electrical signal not  
6        delayed, for forming a third signal by performing an exclusive-OR logic operation upon  
7        said first and second signals, and for detecting a bit rate in dependence upon said third  
8        signal;

9           a clock generator for generating a reference clock signal in dependence upon said  
10      detected bit rate; and

11           a recovery unit for recovering an input clock signal and data from said input  
12      optical signal in dependence upon said reference clock signal;

13           said identification unit comprising:

14           a first unit for delaying said original electrical signal, for performing said  
15      exclusive-OR operation upon said first and second signals, and for forming said third

16 signal; and

17 a second unit for detecting said bit rate of said original signal by low-pass filtering  
18 said third signal, and by deriving said bit rate directly from a voltage level of said low-  
19 pass filtered third signal and without using a phase locked loop; and

20 said clock generator comprising a plurality of oscillators for generating clocking  
21 signals of different frequencies and for selectively operating said oscillators to generate  
22 said reference clock signal in dependence upon said bit rate detected by said  
23 identification unit.

Claim 29. (Canceled)

1 30. (Previously Presented) The apparatus of claim 28, said input optical signal  
2 comprising a plurality of input optical signals, said recovering of said input clock signal  
3 and data from said input optical signal being performed for each of said plurality of input  
4 optical signals, said plurality of input optical signals received having a plurality of  
5 different bit rates.

1 31. (Previously Presented) The apparatus of claim 30, said converter comprising  
2 an optoelectric converter.

1 32. (Previously Presented) The apparatus of claim 31, said identification unit

2 comprising a bit rate identification unit.

Claim 33. (Cancelled)

1 34. (Previously Presented) The apparatus of claim 28, said second unit  
2 comprising:

3 a low-pass filter for low-pass filtering said third signal;

4 an analog-to-digital converter for receiving said low-pass filtered third signal, and  
5 for converting said low-pass filtered third signal from an analog signal to a digital signal;  
6 and

7 a determiner for determining said bit rate in dependence upon said digital signal  
8 received from said analog-to-digital converter.

1 35. (Previously Presented) The apparatus of claim 28, said first unit comprising:

2 a buffer unit for receiving said original electrical signal, and for outputting two  
3 duplicate signals substantially equivalent to said original electrical signal, said two  
4 duplicate signals comprising a primary signal and a secondary signal;

5 a delay unit for receiving said primary signal, for delaying said primary signal by  
6 said predetermined quantity of time, and for outputting said primary signal, said delayed  
7 primary signal comprising said first signal; and

8 an operator unit for performing said exclusive-OR logic operation upon said first

9 and second signals.

Claims 36 - 40. (Canceled)

1 41. (Previously Presented) The apparatus of claim 1, wherein said recovery unit  
2 comprises a programmable recovery unit.

1 42. (Previously Presented) The method of claim 17, wherein said recovery step is  
2 performed by a programmable recovery unit.

1 43. (Previously Presented) The apparatus of claim 28, wherein said recovery unit  
2 comprises a programmable recovery unit.